FIELD PROGRAMMABLE LOGIC ARRAY BASED CASCADABLE N-BIT MAGNITUDE COMPARATOR

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ABSTRACT

This paper is an analytical presentation of the design of an n-bit cascadable digital magnitude comparator (CDMC). The combination of three or more CDMCs in series in some possible problem situations suffers significantly in propagation delay. To minimize this, substantial research efforts have been devoted to developing CDMC using different approaches. This work proposes to use field programmable logic array (FPLA) in the realization of CDCM. Starting from the entered variable (EV) truth-table of the considered 4-bit CDMC case study, a reduced second-order EV Karnaugh map (K-Map) is analyzed based on gate minimum cover to obtain the sum of product (SOP) output expressions of the CDMC. The generalized output expression for n-bit CDMC is then deduced. The unique product-terms (p-term) of the minimum output expressions are used to construct a p-term table which, are consequently used to programme the FPLA which behaves as a CDMC. A symbolic representation of $8 \times p \times 3$ *CDMC FPLA programmed according to the p-term table is generated. It shows the fusible bit position patterns in both the AND and OR planes.*

Keywords: Cascadable digital magnitude comparator; karnaugh map; entered variable; minimum cover; product-term; propagation delay; FPLA

1 INTRODUCTION

The operation to determine which of two n-bit numbers is larger or if they are equal can be performed by a CDMC. It is a fundamental operation in almost all digital processors. CDMC applications are expanding rapidly in modern times because they generate correct signals with high level of reliability [1]. It plays important roles in graphics, data storage operation, as well as the implementation of signal and image processing applications on hardware where the power, speed, and area of an electronic device play a significant role, particularly in the field of modern VLSI technology. An all-optical 1-bit magnitude comparator is proposed using photonic crystal (PhC) waveguide not dependent on nonlinear material. It is based on beam interference principle, using T-shaped lattice with silicon dielectric rods in air background. It is demonstrated through finite-difference time-domain simulation and verified numerically using MATLAB simulation. The size of PhC lattice structure can be as small as 19.167*a* x 19.167*a*, where '*a*' is the lattice constant of the PhC [2]. A hybrid design approach for implementing a two-bit Magnitude Comparator (MC) has been proposed in the work of [3]. This is to enhance high requirement of energy efficient fast circuit designs in modern Integrated Circuits (IC) The hybrid design consists of three different logic techniques namely: (a) Pass Transistor Logic (PTL), (b)

Transmission Gate Logic (TGL) and (c) Conventional Static CMOS Logic (C-CMOS logic). The effectiveness of the proposed design has been compared with 6 state of art two-bit magnitude comparators using Cadence tools in 90nm technology node. The proposed design showed best performance in case of delay and Power Delay Product (PDP) which proved the effectiveness of the design, Moreover, power consumption of the design is also low which makes it highly usable for portable devices that requires low-power consumption. An 18nm FinFET based 2-bit magnitude comparator is the main focus of [4]. FinFET technology is employed to overcome the drawbacks associated with Complementary Metal-Oxide Semiconductor (CMOS) technology like channel length, power consumption, delay and area of transistors, etc. The proposed magnitude comparator is compared to the existing CMOS comparator in terms of power and delay. Power and delay values are calculated and plotted for different values of supply voltage ranging from 0.1-1.0v. LVT (Low Voltage) and HVT (High Voltage) analysis are performed separately. FinFET comparators can be used where fast switching rate is intended, to improve the efficiency of control devices and to make devices compact. It is reported in [5] that NOR logic gate can help in designing of low power, high-speed larger N-bit magnitude comparators. The performance is analysed for power consumption, delay and power-delay product (PDP) with V_{dd} Sweep. The design and simulation are conducted in Cadence Virtuoso Tool environment using 180nm CMOS Technology. The simulation results are in good agreement in terms of power consumption at the percentage of 31.77% and power delay product at the percentage of 35.39%. The Layout is also designed for Proposed Comparator. The implemented circuit has low MOSFET transistor count as compared to basic conventional circuit. This further reduce the area of the chip, which is currently the most important task in the VLSI industry. The challenge of performance of the digital magnitude comparator due to critical path delay created by the internal complexity of the circuit is addressed in [6]. The solution focuses on two novel 1-bit comparator circuits design using CMOS logic structures (combination of pass transistor logic (PTL) and transmission gate logic (TGL)). The 1-bit comparator circuits are compared along with the existing ones. The hybrid exhibits better power delay product (PDP). The simulation results are carried out with the Mentor Graphics tool at V_{dd} = 1V using 22-nm CMOS technology. It is extended to the design and implementation of a 2-bit magnitude comparator. The proposed 2-bit comparator circuit occupies less amount of area on the silicon chip and consumes low power when compared to the existing magnitude comparators. The need for low power design in portable, battery operated and IoT devices is emphasised in the work of [7]. An efficient 2-bit magnitude comparator circuit design is implemented. This technique reduces power consumption, propagation delay, and area of fabrication of digital circuits while maintaining low complexity of logic design when compared to the traditional circuit. The simulations are carried out in Tanner EDA tool. There exists a 12-bit comparator designed using a multiplexer which features small power dissipation and a less area of fabrication. The unique technique involves the use of three 4-bit comparator blocks rather than a single 12-bit comparator to improve speed. However, [8] realized a 2-bit digital comparator based on different logic techniques with a significant improvement in power consumption, propagation delay, and transistor count. Finally, the novel technique has been applied to improve the overall performance of a 12-bit comparator. The simulated results are obtained from EDA tanner tool realized in 32-nanometer technology at 0.7V supply voltage. It shows that the propagation delay of 12-bit digital comparator using the novel technique is 5.15 nanoseconds which is approximately 30% less than the proposed multiplexer-based single 12-bit comparator. In other to improve power efficient, [9] conducted a comparative evaluation of 4-bit digital comparator designed using 2-bit comparator modules with CMOS and low power design techniques viz. AVL, GDI, GDIAVL and the best performing circuit is presented. Two applications of a 4-bit digital comparator are demonstrated to justify the performance of the low power yielding comparator designs. The implementation is done on DSCH 3.5 and simulation on Microwind 3.5 tool on 45nm and 90nm technology. Further comparison between different designs is made in terms of power consumption and other parameters such as leakage current, surface area. In [10], a 32-bit magnitude comparator is designed taken into account of low power, small area and less delay. Full-adder is used in the design of this novel magnitude comparator. Full adder gives two outputs, sum and carry which, is equivalent to the equal to and less than, outputs respectively of the comparator. The design and analysis of a CMOS based efficient

1-bit comparator circuit is presented in [11]. The comparator is designed and simulated based on 180nm TSMC technology. The implemented circuit uses a XNOR gate, two AND gates and two NOT gates. Stacking technique has been used to improve the conventional design. Power supply is varied from 1.0V to 2.8V for the proposed and basic design. Result reflects that the approach shows less power consumption and improved power delay product (PDP). It is stated in [1] that digital comparator with a greater number of bits plays an important role in image processing applications. A speed-optimized and area efficient 32-bit comparator is the focus of this paper. The comparator based on a modified priority encoder technique. The obtained simulation result shows that the area of proposed 32-bit digital comparator consumes 573.73 units which are 20% better when compared to the conventional comparators and the speed improved by 50% when compared with the conventional comparators. The proposed implementation is simulated on the 'Encounter(R) RTL Compiler RC14.28'. The work of [12] proposes to use majority gates which, is one of the natural logic elements of several beyond-CMOS emerging nanotechnologies to design a magnitude comparator. An efficient majority logic implementation of magnitude comparator is highly required to expand the area of application of magnitude comparator. The implementation of majority logic magnitude comparators has lower circuit and delay complexity compared against the already published majority logic magnitude comparator designs. The paper by [13] analyses an n-bit comparator in the general case of arbitrary n and visualizes the analysis for $n = 4$ on a regular and modular version of the 8-variable Karnaugh-map. The cases n = 3, 2 and 1 appear as special cases on 6-variable, 4-variable, and 2-variable submaps of the original map. The analysis is a tutorial exposition of many important concepts in switching theory including those of implicants, prime implicants, essential prime implicants, irredundant disjunctive forms, minimal sums, the complete sum and disjoint sums of products (or probability-ready expressions).

2 CASCADABLE DIGITAL MAGNITUDE COMPARATOR

An n-bit comparator with cascading capability is depicted in Figure 1. The gt input and $(A > B)$ output represent A greater than B; eq and $(A = B)$ represent A equal to B; lt and $(A < B)$ represent A less than B. Cascading ability is realised when the inputs gt, eq, and lt to the kth stage are the outputs ($A > B, A = B$, and $A < B$) from the next least significant ($(k-1)th$ stage. Also, the corresponding outputs of the kth stage are the inputs (gt, eq, and lt) to the next most significant ($(k+1)th$ stage [14].

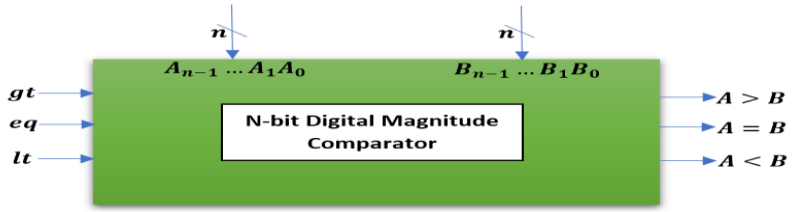


Figure 1. Block diagram of CDMC

2.1 1-bit Cascadable Digital Magnitude Comparator

In the design of CDMC, 1-bit consideration is a good starting point. [14] presents an EV truth-table and EV K-Maps for a 1-bit CDMC as shown in Figure 2.

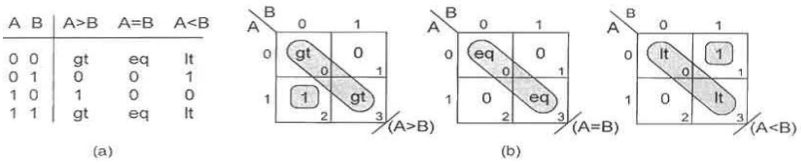


Figure 2. Design of a cascadable 1-bit comparator. (a) Compressed truth table. (b) EV K-Maps plotted from (a) showing minimum cover involving XOR-type functions [14]

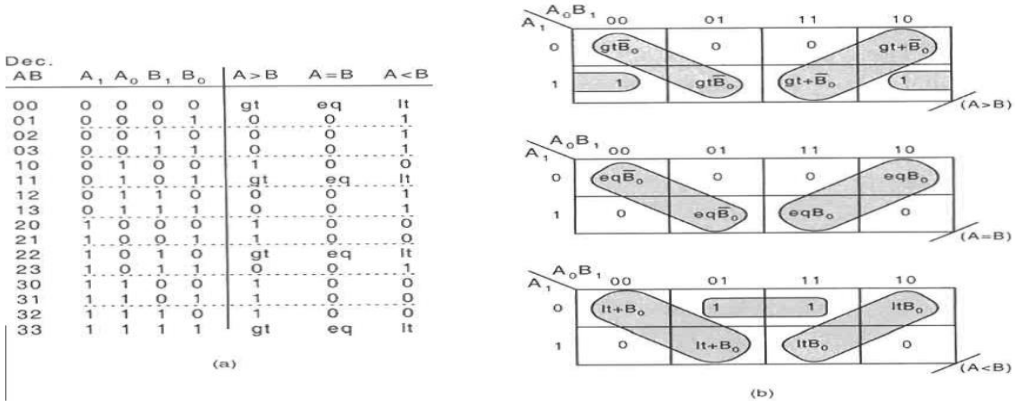
The EV variables gt, eq, and lt in the truth-table appear only when A and B are of equal magnitude. Logic 1 appears when either A or B dominates in magnitude [14]. The gate-minimum output expressions are;

$$\begin{Bmatrix} (A > B) = gt\overline{(A \oplus B)} + A\bar{B} \\ (A = B) = eq\overline{(A \oplus B)} \\ (A < B) = lt\overline{(A \oplus B)} + \bar{A}B \end{Bmatrix} \quad (1)$$

A gate/input tally of 8/16 is obtained, excluding inverter.

2.2 *2-bit Cascadable Digital Magnitude Comparator*

Shown in Figure 3 is the constructed EV truth-table and EV K-Maps for a 2-bit CDMC according to [14]. The EV variables gt, eq, and lt are the outputs from the next least significant stage which, explains why they appear only when A and B are of equal magnitude.



Dec. AB	A_1	A_0	B_1	B_0	A>B	A=B	A<B
00	0	0	0	0	gt	eq	lt
01	0	0	0	1	0	0	1
02	0	0	1	0	0	0	1
03	0	0	1	1	0	0	1
10	0	1	0	0	1	0	0
11	0	1	0	1	gt	eq	lt
12	0	1	1	0	0	0	1
13	0	1	1	1	0	0	1
20	1	0	0	0	1	0	0
21	1	0	0	1	1	0	0
22	1	0	1	0	gt	eq	lt
23	1	0	1	1	0	0	1
30	1	1	0	0	1	0	0
31	1	1	0	1	1	0	0
32	1	1	1	0	1	0	0
33	1	1	1	1	gt	eq	lt

(a)

Figure 3. Design of a cascadable 2-bit comparator. (a) Compressed truth table. (b) EV K-Maps plotted from (a) showing minimum cover involving XOR-type functions [14]

The minimum outputs are;

$$\begin{Bmatrix} (A > B) = gt\{\overline{(A_0 \oplus B_0)}\,\overline{(A_1 \oplus B_1)}\} + A_0\bar{B}_0\{\overline{(A_1 \oplus B_1)}\} + A_1\bar{B}_1 \\ (A = B) = eq\{\overline{(A_0 \oplus B_0)}\,\overline{(A_1 \oplus B_1)}\} \\ (A < B) = lt\{\overline{(A_0 \oplus B_0)}\,\overline{(A_1 \oplus B_1)}\} + \bar{A}_0B_0\{\overline{(A_1 \oplus B_1)}\} + \bar{A}_0B_0 \end{Bmatrix} \quad (2)$$

3 METHODOLOGY

Advances in semiconductor technology and electronics in recent years have led to the rapid development of CDMC. The method proposed in this paper is presented as follows.

3.1 Entered Variable Truth table

The analysis of n-bit CDMC is approached by first studying a 4-bit CDMC. The behavior of 4-bit CDMC is depicted in the EV truth table of Figure 4.

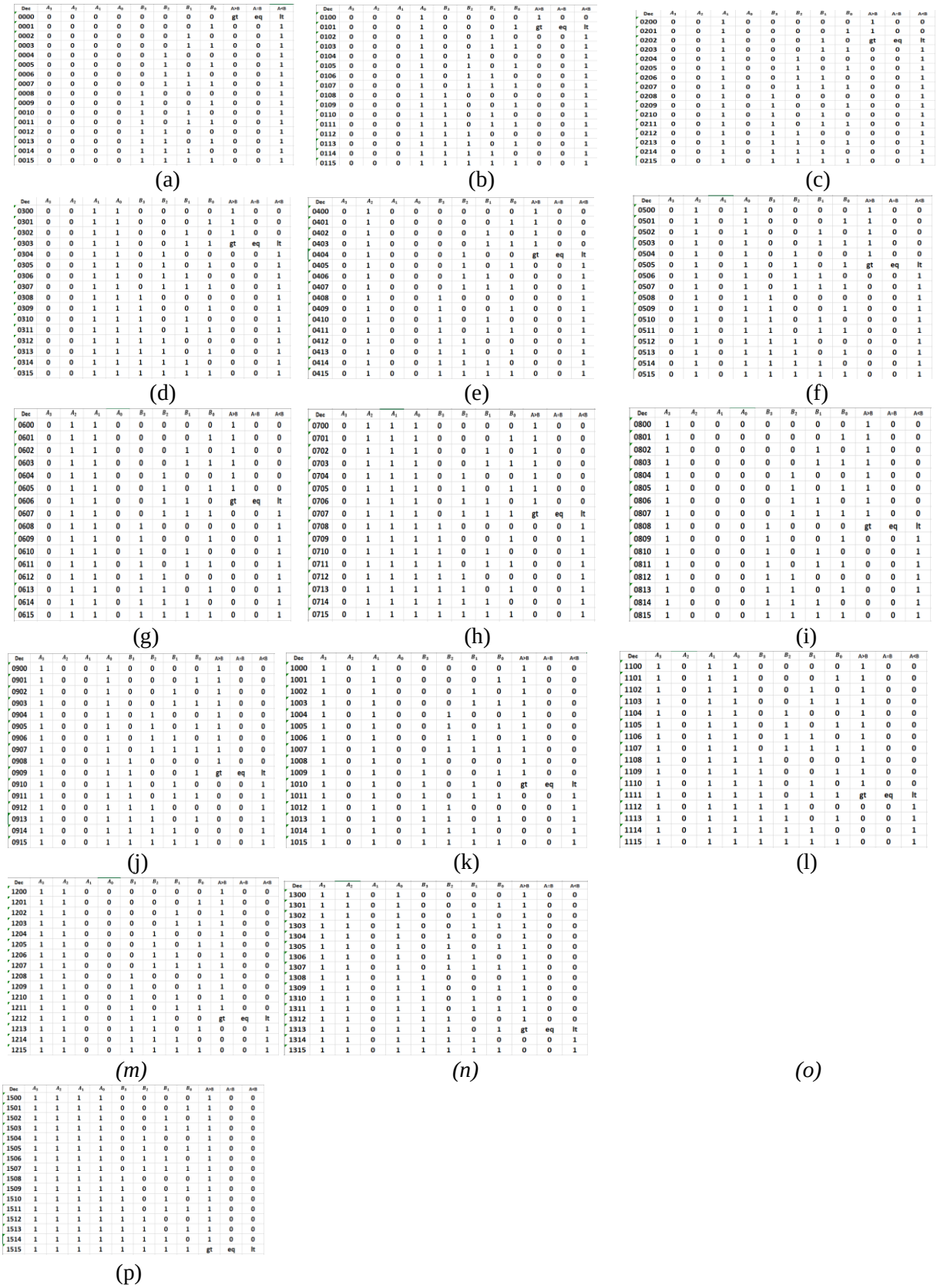


Figure 4. Truth table of 4-bit magnitude comparator

3.2 Generation of Fourth-Order Entered Variable Karnaugh Map

Case 1: $A > B$: Using $A > B$ column of Figure 4 and considering the cells of a fourth-order entered-variable (EV) Karnaugh map (K-Map) shown in Figure 5, based on the pattern, $Cell_{A_3A_2A_1A_0}$, we have the following;

A_3A_2 \ A_1A_0	00	01	11	10
00	$Cell_{0000}$	$Cell_{0001}$	$Cell_{0011}$	$Cell_{0010}$
01	$Cell_{0100}$	$Cell_{0101}$	$Cell_{0111}$	$Cell_{0110}$
11	$Cell_{1100}$	$Cell_{1101}$	$Cell_{1111}$	$Cell_{1110}$
10	$Cell_{1000}$	$Cell_{1001}$	$Cell_{1011}$	$Cell_{1110}$

A>B

Figure 5. Fourth-order EV K-Map of $A > B$. A cell is described as $A_3A_2A_1A_0$

The content of each cell is generated as follows;

$$Cell_{0000} = gt\bar{B}_3\bar{B}_2\bar{B}_1\bar{B}_0 \quad (3)$$

$$Cell_{0001} = \bar{B}_3\bar{B}_2\bar{B}_1\bar{B}_0 + \bar{B}_3\bar{B}_2\bar{B}_1B_0gt = \bar{B}_3\bar{B}_2\bar{B}_1(gtB_0 + \bar{B}_0) = \bar{B}_3\bar{B}_2\bar{B}_1gt + \bar{B}_3\bar{B}_2\bar{B}_1\bar{B}_0 \quad (4)$$

$$Cell_{0010} = \bar{B}_3\bar{B}_2\bar{B}_1 + gt\bar{B}_3\bar{B}_2B_1\bar{B}_0 \quad (5)$$

$$Cell_{0011} = \bar{B}_3\bar{B}_2\bar{B}_1\bar{B}_0 + \bar{B}_3\bar{B}_2\bar{B}_1B_0 + \bar{B}_3\bar{B}_2B_1\bar{B}_0 + gt\bar{B}_3\bar{B}_2B_1B_0 = \bar{B}_3\bar{B}_2\bar{B}_1\bar{B}_0 + \bar{B}_3\bar{B}_2(B_1\oplus B_0) + gt\bar{B}_3\bar{B}_2B_1B_0 \quad (6)$$

$$Cell_{0100} = \bar{B}_3\bar{B}_2\bar{B}_1\bar{B}_0 + \bar{B}_3\bar{B}_2\bar{B}_1B_0 + \bar{B}_3\bar{B}_2B_1\bar{B}_0 + \bar{B}_3\bar{B}_2B_1B_0 + gt\bar{B}_3B_2\bar{B}_1\bar{B}_0 = \bar{B}_3\bar{B}_2(\overline{B_1\oplus B_0}) + \bar{B}_3\bar{B}_2(B_1\oplus B_0) + gt\bar{B}_3B_2\bar{B}_1\bar{B}_0 \quad (7)$$

$$Cell_{0101} = \bar{B}_3\bar{B}_2\bar{B}_1\bar{B}_0 + \bar{B}_3\bar{B}_2\bar{B}_1B_0 + \bar{B}_3\bar{B}_2B_1\bar{B}_0 + \bar{B}_3\bar{B}_2B_1B_0 + \bar{B}_3B_2\bar{B}_1\bar{B}_0 + gt\bar{B}_3B_2\bar{B}_1B_0 = \bar{B}_3\bar{B}_2(\overline{B_1\oplus B_0}) + \bar{B}_3\bar{B}_2(B_1\oplus B_0) + \bar{B}_3B_2\bar{B}_1\bar{B}_0 + gt\bar{B}_3B_2\bar{B}_1B_0 \quad (8)$$

$$Cell_{0110} = \bar{B}_3\bar{B}_2\bar{B}_1\bar{B}_0 + \bar{B}_3\bar{B}_2\bar{B}_1B_0 + \bar{B}_3\bar{B}_2B_1\bar{B}_0 + \bar{B}_3\bar{B}_2B_1B_0 + \bar{B}_3B_2\bar{B}_1\bar{B}_0 + \bar{B}_3B_2\bar{B}_1B_0 + gt\bar{B}_3B_2B_1\bar{B}_0 = \bar{B}_3\bar{B}_2(\overline{B_1\oplus B_0}) + \bar{B}_3\bar{B}_2(B_1\oplus B_0) + \bar{B}_3B_2\bar{B}_1 + gt\bar{B}_3B_2B_1\bar{B}_0 \quad (9)$$

$$Cell_{0111} = \bar{B}_3\bar{B}_2\bar{B}_1\bar{B}_0 + \bar{B}_3\bar{B}_2\bar{B}_1B_0 + \bar{B}_3\bar{B}_2B_1\bar{B}_0 + \bar{B}_3\bar{B}_2B_1B_0 + \bar{B}_3B_2\bar{B}_1\bar{B}_0 + \bar{B}_3B_2\bar{B}_1B_0 + \bar{B}_3B_2B_1\bar{B}_0 + gt\bar{B}_3B_2B_1B_0 = \bar{B}_3\bar{B}_2(\overline{B_1\oplus B_0}) + \bar{B}_3\bar{B}_2(B_1\oplus B_0) + \bar{B}_3B_2(B_1\oplus B_0) + \bar{B}_3B_2\bar{B}_1\bar{B}_0 + gt\bar{B}_3B_2B_1B_0 \quad (10)$$

$$Cell_{1000} = \bar{B}_3\bar{B}_2\bar{B}_1\bar{B}_0 + \bar{B}_3\bar{B}_2\bar{B}_1B_0 + \bar{B}_3\bar{B}_2B_1\bar{B}_0 + \bar{B}_3\bar{B}_2B_1B_0 + \bar{B}_3B_2\bar{B}_1\bar{B}_0 + \bar{B}_3B_2\bar{B}_1B_0 + \bar{B}_3B_2B_1\bar{B}_0 + \bar{B}_3B_2B_1B_0 + gtB_3\bar{B}_2\bar{B}_1\bar{B}_0 = \bar{B}_3\bar{B}_2(\overline{B_1\oplus B_0}) + \bar{B}_3\bar{B}_2(B_1\oplus B_0) + \bar{B}_3B_2(B_1\oplus B_0) + \bar{B}_3B_2(\overline{B_1\oplus B_0}) + gtB_3\bar{B}_2\bar{B}_1\bar{B}_0 \quad (11)$$

$$Cell_{1001} = \bar{B}_3\bar{B}_2\bar{B}_1\bar{B}_0 + \bar{B}_3\bar{B}_2\bar{B}_1B_0 + \bar{B}_3\bar{B}_2B_1\bar{B}_0 + \bar{B}_3\bar{B}_2B_1B_0 + \bar{B}_3B_2\bar{B}_1\bar{B}_0 + \bar{B}_3B_2\bar{B}_1B_0 + \bar{B}_3B_2B_1\bar{B}_0 + \bar{B}_3B_2B_1B_0 + B_3\bar{B}_2\bar{B}_1\bar{B}_0 + gtB_3\bar{B}_2\bar{B}_1B_0 = \bar{B}_3\bar{B}_2(\overline{B_1\oplus B_0}) + \bar{B}_3\bar{B}_2(B_1\oplus B_0) + \bar{B}_3B_2(B_1\oplus B_0) + \bar{B}_3B_2(\overline{B_1\oplus B_0}) + B_3\bar{B}_2\bar{B}_1\bar{B}_0 + gtB_3\bar{B}_2\bar{B}_1B_0 \quad (12)$$

$$Cell_{1010} = \bar{B}_3\bar{B}_2\bar{B}_1\bar{B}_0 + \bar{B}_3\bar{B}_2\bar{B}_1B_0 + \bar{B}_3\bar{B}_2B_1\bar{B}_0 + \bar{B}_3\bar{B}_2B_1B_0 + \bar{B}_3B_2\bar{B}_1\bar{B}_0 + \bar{B}_3B_2\bar{B}_1B_0 + \bar{B}_3B_2B_1\bar{B}_0 + \bar{B}_3B_2B_1B_0 + B_3\bar{B}_2\bar{B}_1\bar{B}_0 + B_3\bar{B}_2\bar{B}_1B_0 + gtB_3\bar{B}_2B_1\bar{B}_0 = \bar{B}_3\bar{B}_2(\overline{B_1\oplus B_0}) + \bar{B}_3\bar{B}_2(B_1\oplus B_0) + \bar{B}_3B_2(B_1\oplus B_0) + \bar{B}_3B_2(\overline{B_1\oplus B_0}) + B_3\bar{B}_2\bar{B}_1 + gtB_3\bar{B}_2B_1\bar{B}_0 \quad (13)$$

$$Cell_{1011} = \bar{B}_3\bar{B}_2\bar{B}_1\bar{B}_0 + \bar{B}_3\bar{B}_2\bar{B}_1B_0 + \bar{B}_3\bar{B}_2B_1\bar{B}_0 + \bar{B}_3\bar{B}_2B_1B_0 + \bar{B}_3B_2\bar{B}_1\bar{B}_0 + \bar{B}_3B_2\bar{B}_1B_0 + \bar{B}_3B_2B_1\bar{B}_0 + B_3\bar{B}_2\bar{B}_1\bar{B}_0 + B_3\bar{B}_2\bar{B}_1B_0 + B_3\bar{B}_2B_1\bar{B}_0 + gtB_3\bar{B}_2B_1B_0 = \bar{B}_3\bar{B}_2(\overline{B_1 \oplus B_0}) + \bar{B}_3B_2(B_1 \oplus B_0) + \bar{B}_2B_3(B_1 \oplus B_0) + B_2\bar{B}_3(\overline{B_1 \oplus B_0}) + B_3\bar{B}_2(B_1 \oplus B_0) + B_3\bar{B}_2\bar{B}_1\bar{B}_0 + gtB_3\bar{B}_2B_1B_0 \quad (14)$$

$$Cell_{1100} = \bar{B}_3\bar{B}_2\bar{B}_1\bar{B}_0 + \bar{B}_3\bar{B}_2\bar{B}_1B_0 + \bar{B}_3\bar{B}_2B_1\bar{B}_0 + \bar{B}_3\bar{B}_2B_1B_0 + \bar{B}_3B_2\bar{B}_1\bar{B}_0 + \bar{B}_3B_2\bar{B}_1B_0 + \bar{B}_3B_2B_1\bar{B}_0 + B_3\bar{B}_2\bar{B}_1\bar{B}_0 + B_3\bar{B}_2\bar{B}_1B_0 + B_3\bar{B}_2B_1\bar{B}_0 + B_3B_2\bar{B}_1\bar{B}_0 = \bar{B}_3\bar{B}_2(\overline{B_1 \oplus B_0}) + \bar{B}_3B_2(B_1 \oplus B_0) + \bar{B}_2B_3(B_1 \oplus B_0) + B_2\bar{B}_3(\overline{B_1 \oplus B_0}) + B_3\bar{B}_2(B_1 \oplus B_0) + B_2\bar{B}_3(\overline{B_1 \oplus B_0}) + gtB_3B_2\bar{B}_1\bar{B}_0 \quad (15)$$

$$Cell_{1101} = \bar{B}_3\bar{B}_2\bar{B}_1\bar{B}_0 + \bar{B}_3\bar{B}_2\bar{B}_1B_0 + \bar{B}_3\bar{B}_2B_1\bar{B}_0 + \bar{B}_3\bar{B}_2B_1B_0 + \bar{B}_3B_2\bar{B}_1\bar{B}_0 + \bar{B}_3B_2\bar{B}_1B_0 + \bar{B}_3B_2B_1\bar{B}_0 + B_3\bar{B}_2\bar{B}_1\bar{B}_0 + B_3\bar{B}_2\bar{B}_1B_0 + B_3\bar{B}_2B_1\bar{B}_0 + B_3B_2\bar{B}_1\bar{B}_0 + gtB_3B_2\bar{B}_1B_0 = \bar{B}_3\bar{B}_2(\overline{B_1 \oplus B_0}) + \bar{B}_3\bar{B}_2(B_1 \oplus B_0) + \bar{B}_2B_3(B_1 \oplus B_0) + \bar{B}_3B_2(\overline{B_1 \oplus B_0}) + B_3\bar{B}_2(B_1 \oplus B_0) + B_2\bar{B}_3(\overline{B_1 \oplus B_0}) + B_3B_2\bar{B}_1\bar{B}_0 + gtB_3B_2\bar{B}_1B_0 \quad (16)$$

$$Cell_{1110} = \bar{B}_3\bar{B}_2\bar{B}_1\bar{B}_0 + \bar{B}_3\bar{B}_2\bar{B}_1B_0 + \bar{B}_3\bar{B}_2B_1\bar{B}_0 + \bar{B}_3\bar{B}_2B_1B_0 + \bar{B}_3B_2\bar{B}_1\bar{B}_0 + \bar{B}_3B_2\bar{B}_1B_0 + \bar{B}_3B_2B_1\bar{B}_0 + B_3\bar{B}_2\bar{B}_1\bar{B}_0 + B_3\bar{B}_2\bar{B}_1B_0 + B_3\bar{B}_2B_1\bar{B}_0 + B_3B_2\bar{B}_1\bar{B}_0 + B_3B_2\bar{B}_1B_0 + gtB_3B_2B_1B_0 = \bar{B}_3\bar{B}_2(\overline{B_1 \oplus B_0}) + \bar{B}_3\bar{B}_2(B_1 \oplus B_0) + \bar{B}_2B_3(B_1 \oplus B_0) + \bar{B}_3B_2(\overline{B_1 \oplus B_0}) + B_3\bar{B}_2(B_1 \oplus B_0) + B_2\bar{B}_3(\overline{B_1 \oplus B_0}) + B_3B_2\bar{B}_1 + gtB_3B_2B_1B_0 \quad (17)$$

$$Cell_{1111} = \bar{B}_3\bar{B}_2\bar{B}_1\bar{B}_0 + \bar{B}_3\bar{B}_2\bar{B}_1B_0 + \bar{B}_3\bar{B}_2B_1\bar{B}_0 + \bar{B}_3\bar{B}_2B_1B_0 + \bar{B}_3B_2\bar{B}_1\bar{B}_0 + \bar{B}_3B_2\bar{B}_1B_0 + \bar{B}_3B_2B_1\bar{B}_0 + B_3\bar{B}_2\bar{B}_1\bar{B}_0 + B_3\bar{B}_2\bar{B}_1B_0 + B_3\bar{B}_2B_1\bar{B}_0 + B_3B_2\bar{B}_1\bar{B}_0 + B_3B_2\bar{B}_1B_0 + B_3B_2B_1\bar{B}_0 + gtB_3B_2B_1B_0 = \bar{B}_3\bar{B}_2(\overline{B_1 \oplus B_0}) + \bar{B}_3\bar{B}_2(B_1 \oplus B_0) + \bar{B}_2B_3(B_1 \oplus B_0) + \bar{B}_3B_2(\overline{B_1 \oplus B_0}) + B_3\bar{B}_2(B_1 \oplus B_0) + B_2\bar{B}_3(\overline{B_1 \oplus B_0}) + B_3B_2(B_1 \oplus B_0)\bar{B}_1\bar{B}_0 + B_3B_2\bar{B}_1\bar{B}_0 + gtB_3B_2B_1B_0 \quad (18)$$

Case II: A = B: Using $A = B$ column of Figure 4, the expressions for the cells of a fourth-order K-Map are shown in Figure 6.

A_3A_2 \ A_1A_0	00	01	11	10
00	$eq\bar{B}_3\bar{B}_2\bar{B}_1\bar{B}_0$	$eq\bar{B}_3\bar{B}_2\bar{B}_1B_0$	$eq\bar{B}_3\bar{B}_2B_1B_0$	$eq\bar{B}_3\bar{B}_2B_1\bar{B}_0$
01	$eq\bar{B}_3B_2\bar{B}_1\bar{B}_0$	$eq\bar{B}_3B_2\bar{B}_1B_0$	$eq\bar{B}_3B_2B_1B_0$	$eq\bar{B}_3B_2B_1\bar{B}_0$
11	$eqB_3B_2\bar{B}_1\bar{B}_0$	$eqB_3B_2\bar{B}_1B_0$	$eqB_3B_2B_1B_0$	$eqB_3B_2B_1\bar{B}_0$
10	$eqB_3\bar{B}_2\bar{B}_1\bar{B}_0$	$eqB_3\bar{B}_2\bar{B}_1B_0$	$eqB_3\bar{B}_2B_1B_0$	$eqB_3\bar{B}_2B_1\bar{B}_0$

A=B

Figure 6. Fourth-order EV K-Map of $A = B$. A cell is described as $A_3A_2A_1A_0$

Case III: A < B: Consider the cells of a fourth-order EV K-Map shown in Figure 7, based on the pattern, $Cell_{A_3A_2A_1A_0}$, we have the following;

A_3A_2 \ A_1A_0	00	01	11	10
00	$Cell_{0000}$	$Cell_{0001}$	$Cell_{0011}$	$Cell_{0010}$
01	$Cell_{0100}$	$Cell_{0101}$	$Cell_{0111}$	$Cell_{0110}$
11	$Cell_{1100}$	$Cell_{1101}$	$Cell_{1111}$	$Cell_{1110}$
10	$Cell_{1000}$	$Cell_{1001}$	$Cell_{1011}$	$Cell_{1110}$

A<B

Figure 7. Fourth-order EV K-Map of $A < B$. A cell is described as $A_3A_2A_1A_0$

The content of each cell is calculated in the following ways;

$$Cell_{0000} = lt\bar{B}_3\bar{B}_2\bar{B}_1\bar{B}_0 + \bar{B}_3\bar{B}_2\bar{B}_1B_0 + \bar{B}_3\bar{B}_2B_1\bar{B}_0 + \bar{B}_3\bar{B}_2B_1B_0 + \bar{B}_3B_2\bar{B}_1\bar{B}_0 + \bar{B}_3B_2\bar{B}_1B_0 + \bar{B}_3B_2B_1\bar{B}_0 + \bar{B}_3B_2B_1B_0 + B_3\bar{B}_2\bar{B}_1\bar{B}_0 + B_3\bar{B}_2\bar{B}_1B_0 + B_3\bar{B}_2B_1\bar{B}_0 + B_3\bar{B}_2B_1B_0 + B_3B_2\bar{B}_1\bar{B}_0 + B_3B_2\bar{B}_1B_0 + B_3B_2B_1\bar{B}_0 + B_3B_2B_1B_0 = lt\bar{B}_3\bar{B}_2\bar{B}_1\bar{B}_0 + \bar{B}_3\bar{B}_2(B_1 \oplus B_0) + \bar{B}_3\bar{B}_2B_1B_0 + \bar{B}_3B_2(B_1 \oplus B_0) + \bar{B}_3B_2(\overline{B_1 \oplus B_0}) + B_3\bar{B}_2(B_1 \oplus B_0) + B_3\bar{B}_2(\overline{B_1 \oplus B_0}) + B_3B_2(B_1 \oplus B_0) + B_3B_2(\overline{B_1 \oplus B_0}) \quad (19)$$

$$Cell_{0001} = lt\bar{B}_3\bar{B}_2\bar{B}_1B_0 + \bar{B}_3\bar{B}_2B_1\bar{B}_0 + \bar{B}_3\bar{B}_2B_1B_0 + \bar{B}_3B_2\bar{B}_1\bar{B}_0 + \bar{B}_3B_2\bar{B}_1B_0 + \bar{B}_3B_2B_1\bar{B}_0 + \bar{B}_3B_2B_1B_0 + B_3\bar{B}_2\bar{B}_1\bar{B}_0 + B_3\bar{B}_2\bar{B}_1B_0 + B_3\bar{B}_2B_1\bar{B}_0 + B_3\bar{B}_2B_1B_0 + B_3B_2\bar{B}_1\bar{B}_0 + B_3B_2\bar{B}_1B_0 + B_3B_2B_1\bar{B}_0 + B_3B_2B_1B_0 = lt\bar{B}_3\bar{B}_2\bar{B}_1B_0 + \bar{B}_3\bar{B}_2B_1 + \bar{B}_3\bar{B}_2(B_1 \oplus B_0) + \bar{B}_3B_2(\overline{B_1 \oplus B_0}) + B_3\bar{B}_2(B_1 \oplus B_0) + B_3\bar{B}_2(\overline{B_1 \oplus B_0}) + B_3B_2(B_1 \oplus B_0) + B_3B_2(\overline{B_1 \oplus B_0}) \quad (20)$$

$$Cell_{0010} = lt\bar{B}_3\bar{B}_2B_1\bar{B}_0 + \bar{B}_3\bar{B}_2B_1B_0 + \bar{B}_3B_2\bar{B}_1\bar{B}_0 + \bar{B}_3B_2\bar{B}_1B_0 + \bar{B}_3B_2B_1\bar{B}_0 + \bar{B}_3B_2B_1B_0 + B_3\bar{B}_2\bar{B}_1\bar{B}_0 + B_3\bar{B}_2\bar{B}_1B_0 + B_3\bar{B}_2B_1\bar{B}_0 + B_3\bar{B}_2B_1B_0 + B_3B_2\bar{B}_1\bar{B}_0 + B_3B_2\bar{B}_1B_0 + B_3B_2B_1\bar{B}_0 + B_3B_2B_1B_0 = lt\bar{B}_3\bar{B}_2B_1\bar{B}_0 + \bar{B}_3\bar{B}_2B_1B_0 + \bar{B}_3B_2(B_1 \oplus B_0) + \bar{B}_3B_2(\overline{B_1 \oplus B_0}) + B_3\bar{B}_2(B_1 \oplus B_0) + B_3\bar{B}_2(\overline{B_1 \oplus B_0}) + B_3B_2(B_1 \oplus B_0) + B_3B_2 \quad (21)$$

$$Cell_{0011} = lt\bar{B}_3\bar{B}_2B_1B_0 + \bar{B}_3B_2\bar{B}_1\bar{B}_0 + \bar{B}_3B_2\bar{B}_1B_0 + \bar{B}_3B_2B_1\bar{B}_0 + \bar{B}_3B_2B_1B_0 + B_3\bar{B}_2\bar{B}_1\bar{B}_0 + B_3\bar{B}_2\bar{B}_1B_0 + B_3\bar{B}_2B_1\bar{B}_0 + B_3\bar{B}_2B_1B_0 + B_3B_2\bar{B}_1\bar{B}_0 + B_3B_2\bar{B}_1B_0 + B_3B_2B_1\bar{B}_0 + B_3B_2B_1B_0 = lt\bar{B}_3\bar{B}_2B_1B_0 + \bar{B}_3B_2(B_1 \oplus B_0) + \bar{B}_3B_2(\overline{B_1 \oplus B_0}) + B_3\bar{B}_2(B_1 \oplus B_0) + B_3\bar{B}_2(\overline{B_1 \oplus B_0}) + B_3B_2(B_1 \oplus B_0) + B_3B_2(\overline{B_1 \oplus B_0}) \quad (22)$$

$$Cell_{0100} = lt\bar{B}_3B_2\bar{B}_1\bar{B}_0 + \bar{B}_3B_2\bar{B}_1B_0 + \bar{B}_3B_2B_1\bar{B}_0 + \bar{B}_3B_2B_1B_0 + B_3\bar{B}_2\bar{B}_1\bar{B}_0 + B_3\bar{B}_2\bar{B}_1B_0 + B_3\bar{B}_2B_1\bar{B}_0 + B_3\bar{B}_2B_1B_0 + B_3B_2\bar{B}_1\bar{B}_0 + B_3B_2\bar{B}_1B_0 + B_3B_2B_1\bar{B}_0 + B_3B_2B_1B_0 = lt\bar{B}_3B_2\bar{B}_1\bar{B}_0 + \bar{B}_3B_2B_1B_0 + \bar{B}_3B_2(B_1 \oplus B_0) + B_3\bar{B}_2(B_1 \oplus B_0) + B_3\bar{B}_2(\overline{B_1 \oplus B_0}) + B_3B_2(B_1 \oplus B_0) + B_3B_2(\overline{B_1 \oplus B_0}) \quad (23)$$

$$Cell_{0101} = lt\bar{B}_3B_2\bar{B}_1B_0 + \bar{B}_3B_2B_1\bar{B}_0 + \bar{B}_3B_2B_1B_0 + B_3\bar{B}_2\bar{B}_1\bar{B}_0 + B_3\bar{B}_2\bar{B}_1B_0 + B_3\bar{B}_2B_1\bar{B}_0 + B_3\bar{B}_2B_1B_0 + B_3B_2\bar{B}_1\bar{B}_0 + B_3B_2\bar{B}_1B_0 + B_3B_2B_1\bar{B}_0 + B_3B_2B_1B_0 = lt\bar{B}_3B_2\bar{B}_1B_0 + \bar{B}_3B_2B_1\bar{B}_0 + \bar{B}_3B_2B_1B_0 + B_3\bar{B}_2(B_1 \oplus B_0) + B_3\bar{B}_2(\overline{B_1 \oplus B_0}) + B_3B_2(B_1 \oplus B_0) + B_3B_2(\overline{B_1 \oplus B_0}) \quad (24)$$

$$Cell_{0110} = lt\bar{B}_3B_2B_1\bar{B}_0 + \bar{B}_3B_2B_1B_0 + B_3\bar{B}_2\bar{B}_1\bar{B}_0 + B_3\bar{B}_2\bar{B}_1B_0 + B_3\bar{B}_2B_1\bar{B}_0 + B_3\bar{B}_2B_1B_0 + B_3B_2\bar{B}_1\bar{B}_0 + B_3B_2\bar{B}_1B_0 + B_3B_2B_1\bar{B}_0 + B_3B_2B_1B_0 = lt\bar{B}_3B_2B_1\bar{B}_0 + \bar{B}_3B_2B_1B_0 + B_3\bar{B}_2(B_1 \oplus B_0) + B_3\bar{B}_2(\overline{B_1 \oplus B_0}) + B_3B_2(B_1 \oplus B_0) + B_3B_2(\overline{B_1 \oplus B_0}) \quad (25)$$

$$Cell_{0111} = lt\bar{B}_3B_2B_1B_0 + B_3\bar{B}_2\bar{B}_1\bar{B}_0 + B_3\bar{B}_2\bar{B}_1B_0 + B_3\bar{B}_2B_1\bar{B}_0 + B_3\bar{B}_2B_1B_0 + B_3B_2\bar{B}_1\bar{B}_0 + B_3B_2\bar{B}_1B_0 + B_3B_2B_1\bar{B}_0 + B_3B_2B_1B_0 = lt\bar{B}_3B_2B_1B_0 + B_3\bar{B}_2(B_1 \oplus B_0) + B_3\bar{B}_2(\overline{B_1 \oplus B_0}) + B_3B_2(B_1 \oplus B_0) + B_3B_2(\overline{B_1 \oplus B_0}) \quad (26)$$

$$Cell_{1000} = lt\bar{B}_3\bar{B}_2\bar{B}_1\bar{B}_0 + B_3\bar{B}_2\bar{B}_1B_0 + B_3\bar{B}_2B_1\bar{B}_0 + B_3\bar{B}_2B_1B_0 + B_3B_2\bar{B}_1\bar{B}_0 + B_3B_2\bar{B}_1B_0 + B_3B_2B_1\bar{B}_0 + B_3B_2B_1B_0 = lt\bar{B}_3\bar{B}_2\bar{B}_1\bar{B}_0 + B_3\bar{B}_2(B_1 \oplus B_0) + B_3\bar{B}_2B_1B_0 + B_3B_2(B_1 \oplus B_0) + B_3B_2(\overline{B_1 \oplus B_0}) \quad (27)$$

$$Cell_{1001} = ltB_3\bar{B}_2\bar{B}_1B_0 + B_3\bar{B}_2B_1\bar{B}_0 + B_3\bar{B}_2B_1B_0 + B_3B_2\bar{B}_1\bar{B}_0 + B_3B_2\bar{B}_1B_0 + B_3B_2B_1\bar{B}_0 + B_3B_2B_1B_0 = ltB_3\bar{B}_2\bar{B}_1B_0 + B_3\bar{B}_2B_1\bar{B}_0 + B_3\bar{B}_2B_1B_0 + B_3B_2(B_1 \oplus B_0) + B_3B_2\overline{(B_1 \oplus B_0)} \quad (28)$$

$$Cell_{1010} = ltB_3\bar{B}_2B_1\bar{B}_0 + B_3\bar{B}_2B_1B_0 + B_3B_2\bar{B}_1\bar{B}_0 + B_3B_2\bar{B}_1B_0 + B_3B_2B_1\bar{B}_0 + B_3B_2B_1B_0 = ltB_3\bar{B}_2B_1\bar{B}_0 + B_3\bar{B}_2B_1B_0 + B_3B_2(B_1 \oplus B_0) + B_3B_2\overline{(B_1 \oplus B_0)} \quad (29)$$

$$Cell_{1011} = ltB_3\bar{B}_2B_1B_0 + B_3B_2\bar{B}_1\bar{B}_0 + B_3B_2\bar{B}_1B_0 + B_3B_2B_1\bar{B}_0 + B_3B_2B_1B_0 = ltB_3\bar{B}_2B_1B_0 + B_3B_2(B_1 \oplus B_0) + B_3B_2\overline{(B_1 \oplus B_0)} \quad (30)$$

$$Cell_{1100} = ltB_3B_2\bar{B}_1\bar{B}_0 + B_3B_2\bar{B}_1B_0 + B_3B_2B_1\bar{B}_0 + B_3B_2B_1B_0 = ltB_3B_2\bar{B}_1\bar{B}_0 + B_3B_2(B_1 \oplus B_0) + B_3B_2B_1B_0 \quad (31)$$

$$Cell_{1101} = ltB_3B_2\bar{B}_1B_0 + B_3B_2B_1\bar{B}_0 + B_3B_2B_1B_0 = ltB_3B_2\bar{B}_1B_0 + B_3B_2B_1\bar{B}_0 + B_3B_2B_1B_0 \quad (32)$$

$$Cell_{1110} = ltB_3B_2B_1\bar{B}_0 + B_3B_2B_1B_0 = ltB_3B_2B_1\bar{B}_0 + B_3B_2B_1B_0 \quad (33)$$

$$Cell_{1111} = ltB_3B_2B_1B_0 \quad (34)$$

3.3 Reduction of Fourth-Order EV K-Map to Second-Order Type

Case 1: $A > B$

The fourth-order EV K-Map of Figure 5 with respect to $A > B$ is further reduced to second-order EV K-Map as follows.

$$(Cell_{0000}, Cell_{0001}, Cell_{0100}, Cell_{0101}) = \bar{A}_3\bar{A}_2\bar{A}_1\bar{A}_0(gt\bar{B}_3\bar{B}_2\bar{B}_1\bar{B}_0) + \bar{A}_3\bar{A}_2\bar{A}_1A_0(\bar{B}_3\bar{B}_2\bar{B}_1B_0gt + \bar{B}_3\bar{B}_2\bar{B}_1\bar{B}_0) + \bar{A}_3A_2\bar{A}_1\bar{A}_0(\bar{B}_3\bar{B}_2\overline{(B_1 \oplus B_0)} + \bar{B}_3\bar{B}_2(B_1 \oplus B_0) + gt\bar{B}_3B_2\bar{B}_1\bar{B}_0) + \bar{A}_3A_2\bar{A}_1A_0(\bar{B}_3\bar{B}_2\overline{(B_1 \oplus B_0)} + \bar{B}_3\bar{B}_2(B_1 \oplus B_0) + \bar{B}_3B_2\bar{B}_1\bar{B}_0 + gt\bar{B}_3B_2\bar{B}_1B_0) \quad (35)$$

$$(Cell_{0011}, Cell_{0010}, Cell_{0111}, Cell_{0110}) = \bar{A}_3\bar{A}_2A_1A_0(\bar{B}_3\bar{B}_2\bar{B}_1\bar{B}_0 + \bar{B}_3\bar{B}_2(B_1 \oplus B_0) + gt\bar{B}_3\bar{B}_2B_1B_0) + \bar{A}_3\bar{A}_2A_1\bar{A}_0(\bar{B}_3\bar{B}_2\bar{B}_1 + gt\bar{B}_3\bar{B}_2B_1\bar{B}_0) + \bar{A}_3A_2A_1A_0(\bar{B}_3\bar{B}_2\overline{(B_1 \oplus B_0)} + \bar{B}_3\bar{B}_2(B_1 \oplus B_0) + \bar{B}_3B_2(B_1 \oplus B_0) + \bar{B}_3B_2\bar{B}_1\bar{B}_0 + gt\bar{B}_3B_2B_1B_0) + \bar{A}_3A_2A_1\bar{A}_0(\bar{B}_3\bar{B}_2\overline{(B_1 \oplus B_0)} + \bar{B}_3\bar{B}_2(B_1 \oplus B_0) + \bar{B}_3B_2\bar{B}_1 + gt\bar{B}_3B_2B_1\bar{B}_0) \quad (36)$$

$$(Cell_{1100}, Cell_{1101}, Cell_{1000}, Cell_{1001}) = A_3A_2\bar{A}_1\bar{A}_0(\bar{B}_3\bar{B}_2\overline{(B_1 \oplus B_0)} + \bar{B}_3\bar{B}_2(B_1 \oplus B_0) + \bar{B}_3B_2(B_1 \oplus B_0) + \bar{B}_3B_2\overline{(B_1 \oplus B_0)} + B_3\bar{B}_2(B_1 \oplus B_0) + B_3\bar{B}_2\overline{(B_1 \oplus B_0)} + gtB_3B_2\bar{B}_1\bar{B}_0) + A_3A_2\bar{A}_1A_0(\bar{B}_3\bar{B}_2\overline{(B_1 \oplus B_0)} + \bar{B}_3\bar{B}_2(B_1 \oplus B_0) + \bar{B}_3B_2(B_1 \oplus B_0) + \bar{B}_3B_2\overline{(B_1 \oplus B_0)} + B_3\bar{B}_2(B_1 \oplus B_0) + B_3\bar{B}_2\overline{(B_1 \oplus B_0)} + B_3B_2\bar{B}_1\bar{B}_0 + gtB_3B_2\bar{B}_1B_0) + A_3\bar{A}_2\bar{A}_1\bar{A}_0(\bar{B}_3\bar{B}_2\overline{(B_1 \oplus B_0)} + \bar{B}_3\bar{B}_2(B_1 \oplus B_0) + \bar{B}_3B_2(B_1 \oplus B_0) + \bar{B}_3B_2\overline{(B_1 \oplus B_0)} + B_3\bar{B}_2(B_1 \oplus B_0) + B_3\bar{B}_2\overline{(B_1 \oplus B_0)} + B_3B_2\bar{B}_1\bar{B}_0 + gtB_3B_2\bar{B}_1B_0) + A_3\bar{A}_2\bar{A}_1A_0(\bar{B}_3\bar{B}_2\overline{(B_1 \oplus B_0)} + \bar{B}_3\bar{B}_2(B_1 \oplus B_0) + \bar{B}_3B_2(B_1 \oplus B_0) + \bar{B}_3B_2\overline{(B_1 \oplus B_0)} + B_3\bar{B}_2\bar{B}_1\bar{B}_0 + gtB_3\bar{B}_2\bar{B}_1B_0) \quad (37)$$

$$(Cell_{1111}, Cell_{1110}, Cell_{1011}, Cell_{1010}) = A_3A_2A_1A_0\left(\bar{B}_3\bar{B}_2(\overline{B_1 \oplus B_0}) + \bar{B}_3\bar{B}_2(B_1 \oplus B_0) + \bar{B}_3B_2(B_1 \oplus B_0) + \bar{B}_3B_2(\overline{B_1 \oplus B_0}) + B_3\bar{B}_2(B_1 \oplus B_0) + B_3\bar{B}_2(\overline{B_1 \oplus B_0}) + B_3B_2(\overline{B_1 \oplus B_0})\bar{B}_1\bar{B}_0 + B_3B_2B_0(gt + \bar{B}_1)\right) + A_3A_2A_1\bar{A}_0(\bar{B}_3\bar{B}_2(\overline{B_1 \oplus B_0}) + \bar{B}_3\bar{B}_2(B_1 \oplus B_0) + \bar{B}_3B_2(B_1 \oplus B_0) + \bar{B}_3B_2(\overline{B_1 \oplus B_0}) + B_3\bar{B}_2(B_1 \oplus B_0) + B_3\bar{B}_2(\overline{B_1 \oplus B_0}) + B_3B_2\bar{B}_1 + gtB_3B_2B_1B_0) + A_3\bar{A}_2A_1A_0(\bar{B}_3\bar{B}_2(\overline{B_1 \oplus B_0}) + \bar{B}_3\bar{B}_2(B_1 \oplus B_0) + \bar{B}_3B_2(B_1 \oplus B_0) + \bar{B}_3B_2(\overline{B_1 \oplus B_0}) + B_3\bar{B}_2(B_1 \oplus B_0) + B_3\bar{B}_2\bar{B}_1\bar{B}_0 + gtB_3\bar{B}_2B_1B_0) + A_3\bar{A}_2A_1\bar{A}_0(\bar{B}_3\bar{B}_2(\overline{B_1 \oplus B_0}) + \bar{B}_3\bar{B}_2(B_1 \oplus B_0) + \bar{B}_3B_2(B_1 \oplus B_0) + \bar{B}_3B_2(\overline{B_1 \oplus B_0}) + B_3\bar{B}_2\bar{B}_1 + gtB_3\bar{B}_2B_1\bar{B}_0) \quad (38)$$

Equation (35) through to (38) were used to fill the cells of the second-order EV K-Map shown in Figure 8.

A_3 \ A_1	0	1
0	$(Cell_{0000}, Cell_{0001}, Cell_{0100}, Cell_{0101})$	$(Cell_{0011}, Cell_{0010}, Cell_{0111}, Cell_{0110})$
1	$(Cell_{1100}, Cell_{1101}, Cell_{1000}, Cell_{1001})$	$(Cell_{1111}, Cell_{1110}, Cell_{1011}, Cell_{1010})$

A > B

Figure 8. Second-order EV K-Map of $(\mathrm{A} > \mathrm{B})$

Further simplification of the K-Map of Figure 8 based on gate-minimum cover yields;

$$(A > B) = gt\{(\overline{A_0 \oplus B_0})(\overline{A_1 \oplus B_1})(\overline{A_2 \oplus B_2})(\overline{A_3 \oplus B_3})\} + A_0\bar{B}_0\{(\overline{A_1 \oplus B_1})(\overline{A_2 \oplus B_2})(\overline{A_3 \oplus B_3})\} + A_1\bar{B}_1\{(\overline{A_2 \oplus B_2})(\overline{A_3 \oplus B_3})\} + A_2\bar{B}_2\{\overline{A_3 \oplus B_3}\} + A_3\bar{B}_3 \quad (39)$$

For an n-bit CDMC, $(A > B)$ is deduced as;

$$(A > B) = gt\{(\overline{A_0 \oplus B_0})(\overline{A_1 \oplus B_1})(\overline{A_2 \oplus B_2})(\overline{A_3 \oplus B_3}) \ldots\ldots (\overline{A_{n-1} \oplus B_{n-1}})\} + A_0\bar{B}_0\{(\overline{A_1 \oplus B_1})(\overline{A_2 \oplus B_2})(\overline{A_3 \oplus B_3}) \ldots\ldots (\overline{A_{n-1} \oplus B_{n-1}})\} + A_1\bar{B}_1\{(\overline{A_2 \oplus B_2})(\overline{A_3 \oplus B_3}) \ldots\ldots (\overline{A_{n-1} \oplus B_{n-1}})\} + \cdots + A_{n-2}\bar{B}_{n-2}\{\overline{A_{n-1} \oplus B_{n-1}}\} + A_{n-1}\bar{B}_{n-1} \quad (40)$$

Rewritting (40) as SOP, it yields

$$(A > B) = \{\overline{gtA_0B_0\bar{A}_0\bar{B}_0 + gtA_1B_1\bar{A}_1\bar{B}_1 + A_2B_2\bar{A}_2\bar{B}_2 + A_3B_3\bar{A}_3\bar{B}_3 + \cdots + A_{n-1}B_{n-1}\bar{A}_{n-1}\bar{B}_{n-1}}\} + \{\overline{A_0\bar{B}_0A_1B_1\bar{A}_1\bar{B}_1 + A_0\bar{B}_0A_2B_2\bar{A}_2\bar{B}_2 + A_3B_3\bar{A}_3\bar{B}_3 + \cdots + A_{n-1}B_{n-1}\bar{A}_{n-1}\bar{B}_{n-1}}\} + \{A_1\bar{B}_1A_2B_2\bar{A}_2\bar{B}_2 + A_1\bar{B}_1A_3B_3\bar{A}_3\bar{B}_3 + \cdots + A_{n-1}B_{n-1}\bar{A}_{n-1}\bar{B}_{n-1}\} + \cdots + \{A_{n-2}\bar{B}_{n-2}A_{n-1}B_{n-1}\bar{A}_{n-1}\bar{B}_{n-1}\} + A_{n-1}\bar{B}_{n-1} \quad (41)$$

Case II: $A = B$: The fourth-order EV K-Map of Figure 6 is reduced to a second-order EV K-Map shown in Figure 9.

$$(Cell_{0000}, Cell_{0001}, Cell_{0100}, Cell_{0101}) = \bar{A}_3\bar{A}_2\bar{A}_1\bar{A}_0(eq\bar{B}_3\bar{B}_2\bar{B}_1\bar{B}_0) + \bar{A}_3\bar{A}_2\bar{A}_1A_0(eq\bar{B}_3\bar{B}_2\bar{B}_1B_0) + \bar{A}_3A_2\bar{A}_1\bar{A}_0(eq\bar{B}_3B_2\bar{B}_1\bar{B}_0) + \bar{A}_3A_2\bar{A}_1A_0(eq\bar{B}_3B_2\bar{B}_1B_0) \quad (42)$$

$$(Cell_{0011}, Cell_{0010}, Cell_{0111}, Cell_{0110}) = \bar{A}_3\bar{A}_2A_1A_0(eq\bar{B}_3\bar{B}_2B_1B_0) + \bar{A}_3\bar{A}_2A_1\bar{A}_0(eq\bar{B}_3\bar{B}_2B_1\bar{B}_0) + \bar{A}_3A_2A_1A_0(eq\bar{B}_3B_2B_1B_0) + \bar{A}_3A_2A_1\bar{A}_0(eq\bar{B}_3B_2B_1\bar{B}_0) \quad (43)$$

$$(Cell_{1100}, Cell_{1101}, Cell_{1000}, Cell_{1001}) = A_3A_2\bar{A}_1\bar{A}_0(eqB_3B_2\bar{B}_1\bar{B}_0) + A_3A_2\bar{A}_1A_0(eqB_3B_2\bar{B}_1B_0) + A_3\bar{A}_2\bar{A}_1\bar{A}_0(eqB_3\bar{B}_2\bar{B}_1\bar{B}_0) + A_3\bar{A}_2\bar{A}_1A_0(eqB_3\bar{B}_2\bar{B}_1B_0) \quad (44)$$

$$(Cell_{1111}, Cell_{1110}, Cell_{1011}, Cell_{1010}) = A_3A_2A_1A_0(eqB_3B_2B_1B_0) + A_3A_2A_1\bar{A}_0(eqB_3B_2B_1\bar{B}_0) + A_3\bar{A}_2A_1A_0(eqB_3\bar{B}_2B_1B_0) + A_3\bar{A}_2A_1\bar{A}_0(eqB_3\bar{B}_2B_1\bar{B}_0) \quad (45)$$

Equation (42) through to (45) are used as contents of cells of Figure 9.

A_3 \ A_1	0	1
0	$(Cell_{0000}, Cell_{0001}, Cell_{0100}, Cell_{0101})$	$(Cell_{0011}, Cell_{0010}, Cell_{0111}, Cell_{0110})$
1	$(Cell_{1100}, Cell_{1101}, Cell_{1000}, Cell_{1001})$	$(Cell_{1111}, Cell_{1110}, Cell_{1011}, Cell_{1010})$

A=B

Figure 9. Second-order EV K-Map of $(\mathrm{A} = \mathrm{B})$

The EV K-Map of Figure 9 simplifies to

$$(A = B) = (\overline{A_0 \oplus B_0})(\overline{A_1 \oplus B_1})(\overline{A_2 \oplus B_2})(\overline{A_3 \oplus B_3}) \quad (46)$$

For an n-bit CDMC, $(A = B)$ is expressed as

$$(A = B) = (\overline{A_0 \oplus B_0})(\overline{A_1 \oplus B_1})(\overline{A_2 \oplus B_2})(\overline{A_3 \oplus B_3}) \ldots\ldots (\overline{A_{n-1} \oplus B_{n-1}})$$

Case III: $A < B$: The fourth-order EV K-Map of Figure 7 with respect to $A < B$ is further reduced to second-order EV K-Map as follows.

$$(Cell_{0000}, Cell_{0001}, Cell_{0100}, Cell_{0101}) = \bar{A}_3\bar{A}_2\bar{A}_1\bar{A}_0\big(lt\bar{B}_3\bar{B}_2\bar{B}_1\bar{B}_0 + \bar{B}_3\bar{B}_2(B_1 \oplus B_0) + \bar{B}_3\bar{B}_2B_1B_0 + \bar{B}_3B_2(B_1 \oplus B_0) + \bar{B}_3B_2(\overline{B_1 \oplus B_0}) + B_3\bar{B}_2(B_1 \oplus B_0) + B_3\bar{B}_2(\overline{B_1 \oplus B_0}) + B_3B_2(B_1 \oplus B_0) + B_3B_2(\overline{B_1 \oplus B_0})\big) + \bar{A}_3\bar{A}_2\bar{A}_1A_0\big(lt\bar{B}_3\bar{B}_2\bar{B}_1B_0 + \bar{B}_3\bar{B}_2B_1 + \bar{B}_3B_2(B_1 \oplus B_0) + \bar{B}_3B_2(\overline{B_1 \oplus B_0}) + B_3\bar{B}_2(B_1 \oplus B_0) + B_3\bar{B}_2(\overline{B_1 \oplus B_0}) + B_3B_2(B_1 \oplus B_0) + B_3B_2(\overline{B_1 \oplus B_0})\big) + \bar{A}_3A_2\bar{A}_1\bar{A}_0\big(lt\bar{B}_3B_2\bar{B}_1B_0 + \bar{B}_3B_2B_1\bar{B}_0 + \bar{B}_3B_2B_1B_0 + B_3\bar{B}_2(B_1 \oplus B_0) + B_3\bar{B}_2(\overline{B_1 \oplus B_0}) + B_3B_2(B_1 \oplus B_0) + B_3B_2(\overline{B_1 \oplus B_0})\big) + \bar{A}_3A_2\bar{A}_1A_0\big(lt\bar{B}_3B_2\bar{B}_1B_0 + \bar{B}_3B_2B_1\bar{B}_0 + \bar{B}_3B_2B_1B_0 + B_3\bar{B}_2(B_1 \oplus B_0) + B_3\bar{B}_2(\overline{B_1 \oplus B_0}) + B_3B_2(B_1 \oplus B_0) + B_3B_2(\overline{B_1 \oplus B_0})\big) \quad (47)$$

$$(Cell_{0011}, Cell_{0010}, Cell_{0111}, Cell_{0110}) = \bar{A}_3\bar{A}_2A_1A_0\big(lt\bar{B}_3\bar{B}_2B_1B_0 + \bar{B}_3B_2(B_1 \oplus B_0) + \bar{B}_3B_2(\overline{B_1 \oplus B_0}) + B_3\bar{B}_2(B_1 \oplus B_0) + B_3\bar{B}_2(\overline{B_1 \oplus B_0}) + B_3B_2(B_1 \oplus B_0) + B_3B_2(\overline{B_1 \oplus B_0})\big) + \bar{A}_3\bar{A}_2A_1\bar{A}_0\big(lt\bar{B}_3\bar{B}_2B_1\bar{B}_0 + \bar{B}_3\bar{B}_2B_1B_0 + \bar{B}_3B_2(B_1 \oplus B_0) + \bar{B}_3B_2(\overline{B_1 \oplus B_0}) + B_3\bar{B}_2(B_1 \oplus B_0) + B_3\bar{B}_2(\overline{B_1 \oplus B_0}) + B_3B_2(B_1 \oplus B_0) + B_3B_2(\overline{B_1 \oplus B_0})\big) + \bar{A}_3A_2A_1A_0\big(lt\bar{B}_3B_2B_1B_0 + B_3\bar{B}_2(B_1 \oplus B_0) + B_3\bar{B}_2(\overline{B_1 \oplus B_0}) + B_3B_2(B_1 \oplus B_0) + B_3B_2(\overline{B_1 \oplus B_0})\big) + \bar{A}_3A_2A_1\bar{A}_0\big(lt\bar{B}_3B_2B_1\bar{B}_0 + \bar{B}_3B_2B_1B_0 + B_3\bar{B}_2(B_1 \oplus B_0) + B_3\bar{B}_2(\overline{B_1 \oplus B_0}) + B_3B_2(B_1 \oplus B_0) + B_3B_2(\overline{B_1 \oplus B_0})\big) \quad (48)$$

$$(Cell_{1100}, Cell_{1101}, Cell_{1000}, Cell_{1001}) = A_3A_2\bar{A}_1\bar{A}_0(lt\bar{B}_3B_2\bar{B}_1\bar{B}_0 + B_3B_2(B_1 \oplus B_0) + B_3B_2B_1B_0) + A_3A_2\bar{A}_1A_0(lt\bar{B}_3B_2\bar{B}_1B_0 + B_3B_2B_1\bar{B}_0 + B_3B_2B_1B_0) + A_3\bar{A}_2\bar{A}_1\bar{A}_0\big(lt\bar{B}_3\bar{B}_2\bar{B}_1\bar{B}_0 + B_3\bar{B}_2(B_1 \oplus B_0) + B_3\bar{B}_2B_1B_0 + B_3B_2(B_1 \oplus B_0) + B_3B_2(\overline{B_1 \oplus B_0})\big) + A_3\bar{A}_2\bar{A}_1A_0\big(lt\bar{B}_3\bar{B}_2\bar{B}_1B_0 + B_3\bar{B}_2B_1\bar{B}_0 + B_3\bar{B}_2B_1B_0 + B_3B_2(B_1 \oplus B_0) + B_3B_2(\overline{B_1 \oplus B_0})\big) \quad (49)$$

$$(Cell_{1111}, Cell_{1110}, Cell_{1011}, Cell_{1010}) = A_3A_2A_1A_0(lt\bar{B}_3B_2B_1B_0) + A_3A_2A_1\bar{A}_0(lt\bar{B}_3B_2B_1\bar{B}_0 + B_3B_2B_1B_0) + A_3\bar{A}_2A_1A_0\big(lt\bar{B}_3\bar{B}_2B_1B_0 + B_3B_2(B_1 \oplus B_0) + B_3B_2(\overline{B_1 \oplus B_0})\big) + A_3\bar{A}_2A_1\bar{A}_0\big(lt\bar{B}_3\bar{B}_2B_1\bar{B}_0 + B_3\bar{B}_2B_1B_0 + B_3B_2(B_1 \oplus B_0) + B_3B_2(\overline{B_1 \oplus B_0})\big) \quad (50)$$

Equation (47) through to (50) are used to fill in the cells of the second-order EV K-Map shown in Figure 10.

A_3 \ A_1	0	1
0	$\begin{matrix}Cell_{0000}, Cell_{0001},\\ Cell_{0100}, Cell_{0101}\end{matrix}$	$\begin{matrix}Cell_{0011}, Cell_{0010},\\ Cell_{0111}, Cell_{0110}\end{matrix}$
1	$\begin{matrix}Cell_{1100}, Cell_{1101},\\ Cell_{1000}, Cell_{1001}\end{matrix}$	$\begin{matrix}Cell_{1111}, Cell_{1110},\\ Cell_{1011}, Cell_{1010}\end{matrix}$

A<B

Figure 10. Second-order EV K-Map of $(A < B)$

The simplification of the EV K-Map of Figure 10 gives;

$$(A < B) = lt\{(\overline{A_0 \oplus B_0})(\overline{A_1 \oplus B_1})(\overline{A_2 \oplus B_2})(\overline{A_3 \oplus B_3})\} + \bar{A}_0 B_0\{(\overline{A_1 \oplus B_1})(\overline{A_2 \oplus B_2})(\overline{A_3 \oplus B_3})\} + \bar{A}_1 B_1\{(\overline{A_2 \oplus B_2})(\overline{A_3 \oplus B_3})\} + \bar{A}_2 B_2\{\overline{A_3 \oplus B_3}\} + \bar{A}_3 B_3 \quad (51)$$

For an n-bit CDMC, $(A < B)$ is expressed as

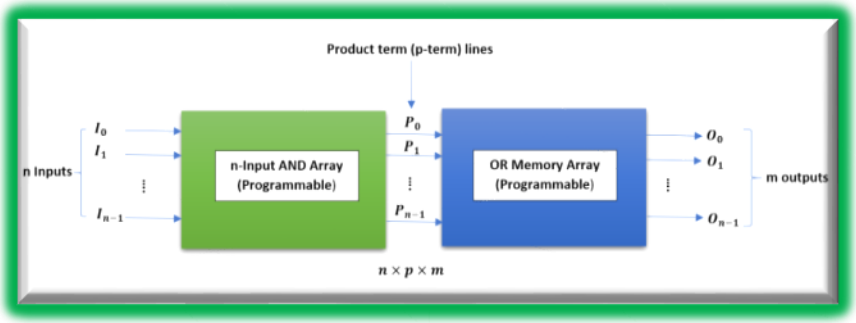
$$(A < B) = lt\{(\overline{A_0 \oplus B_0})(\overline{A_1 \oplus B_1})(\overline{A_2 \oplus B_2})(\overline{A_3 \oplus B_3}) \ldots\ldots (\overline{A_{n-1} \oplus B_{n-1}})\} + \bar{A}_0 B_0\{(\overline{A_1 \oplus B_1})(\overline{A_2 \oplus B_2})(\overline{A_3 \oplus B_3}) \ldots\ldots (\overline{A_{n-1} \oplus B_{n-1}})\} + \bar{A}_1 B_1\{(\overline{A_2 \oplus B_2})(\overline{A_3 \oplus B_3}) \ldots\ldots (\overline{A_{n-1} \oplus B_{n-1}})\} + \cdots + \bar{A}_{n-2} B_{n-2}\{\overline{A_{n-1} \oplus B_{n-1}}\} + \bar{A}_{n-1} B_{n-1} \quad (52)$$

Rewriting (52) as SOP, it yields

$$(A < B) = \{\overline{lt A_0 B_0 \bar{A}_0 \bar{B}_0 + lt A_1 B_1 \bar{A}_1 \bar{B}_1 + A_2 B_2 \bar{A}_2 \bar{B}_2 + A_3 B_3 \bar{A}_3 \bar{B}_3 + \cdots + A_{n-1} B_{n-1} \bar{A}_{n-1} \bar{B}_{n-1}}\} + \{\overline{\bar{A}_0 B_0 A_1 B_1 \bar{A}_1 \bar{B}_1 + \bar{A}_0 B_0 A_2 B_2 \bar{A}_2 \bar{B}_2 + A_3 B_3 \bar{A}_3 \bar{B}_3 + \cdots + A_{n-1} B_{n-1} \bar{A}_{n-1} \bar{B}_{n-1}}\} + \{\overline{\bar{A}_1 B_1 A_2 B_2 \bar{A}_2 \bar{B}_2 + \bar{A}_1 B_1 A_3 B_3 \bar{A}_3 \bar{B}_3 + \cdots + A_{n-1} B_{n-1} \bar{A}_{n-1} \bar{B}_{n-1}}\} + \cdots + \{\overline{\bar{A}_{n-2} B_{n-2} A_{n-1} B_{n-1} \bar{A}_{n-1} \bar{B}_{n-1}}\} + \bar{A}_{n-1} B_{n-1} \quad (53)$$

3.4 Field Programmable Logic Array

FPLA is one of the programmable universal digital logic function implementers, combinational and sequential inclusive. It is an n-input/m-output component consisting of an input ANDing stage and an ORing output stage as in Figure 11. Both stages are programmable as depicted in Figure 12. The p-terms are generated by the AND stage, while the OR stage ORs the appropriate p-terms together to produce the required SOP functions.



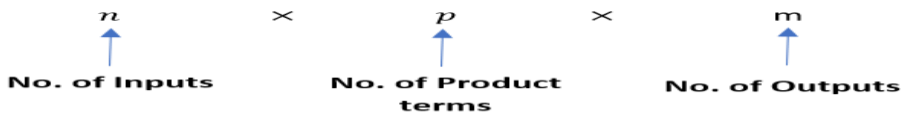


Figure 11. Block diagram for an n-input/m-output FPLA showing the programmable 'AND' and 'OR' stages and the p product-term lines

A FPLA shown in Figure 11 is described using the following dimensionality: The maximum number of unique p-terms a FPLA can accommodate is p. It is masked set and is usually much less than 2^n. There are m possible outputs composed of up to p unique p-terms. In this work, $n = 2(n-1) + 3$, $m = 3$, that is number of outputs.

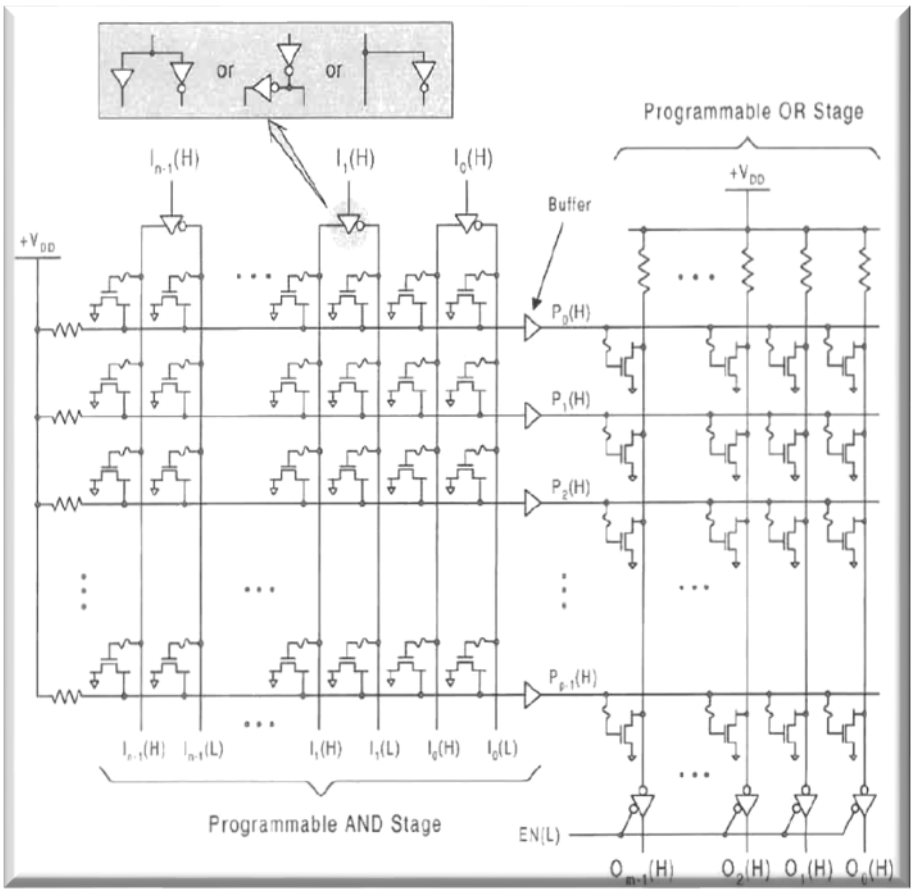


Figure 12. MOS version of an unprogrammed $n \times p \times m$ FPLA showing the programmable NMOS connections for normally active bit locations in the AND and OR (memory) sections, and showing tri-state outputs with active low enable controls [14]

4 RESULTS AND DISCUSSION

Figure 13 is the formulated symbolic representation of an $8 \times p \times 3$ FPLA based implementation of CDMC. It is programmed using the p-term table presented in Table 1. The symbolism that is used avoids the need to provide details of the specific technology used in the FPLA. However, the symbolism is associated with FPLA metal-oxide semiconductor (MOS) technology. The (×) symbol in the AND plane signifies an input to a p-term and represents a disconnected fusible negative MOS (NMOS) link as depicted in Figure 12. The filled square (■) in the OR plane represents the programmed storage of 1(L) by a connected fusible NMOS link as shown in Figure 12, and the empty cross-junctions in the OR plane

indicates the programmed storage of 0(L) created by a disconnected fusible NMOS link. In Figure 13, the representative p-terms are given at the left and adjacent to their respective p-term lines.

Table 1. P-term table for n-bit CDMC

p-Term	Inputs																			Outputs		
	B_{n-1}	B_{n-2}	...	B_n	B_1	B_0	B_0	A_{n-1}	A_{n-2}	...	A_n	A_1	A_2	A_1	A_0	gt	eq	lt	A>B	A=B	A<B
$gtA_1B_0\bar{A}_1\bar{B}_0$	-	-		-	-	-	d	-	-		-	-	-	-	d	1	-	-	1	0	0
$gtA_1B_1\bar{A}_1\bar{B}_1$	-	-		-	-	d	-	-	-		-	-	-	d	-	1	-	-	1	0	0
$A_1B_2\bar{A}_2\bar{B}_2$	-	-		-	-	d	-	-	-		-	-	d	-	-	-	-	-	1	0	0
$A_1B_3\bar{A}_3\bar{B}_3$	-	-		-	d	-	-	-	-		-	d	-	-	-	-	-	-	1	0	0
$A_{n-1}B_{n-1}\bar{A}_{n-1}\bar{B}_{n-1}$	d	-		-	-	-	-	d	-		-	-	-	-	-	-	-	-	1	0	0
$A_0\bar{B}_0A_1B_1\bar{A}_1\bar{B}_1$	-	-		-	-	d	0	-	-		-	-	-	d	1	-	-	-	1	0	0
$A_0\bar{B}_0A_2B_2\bar{A}_2\bar{B}_2$	-	-		-	-	d	0	-	-		-	-	d	-	1	-	-	-	1	0	0
$A_1B_1\bar{A}_1\bar{B}_1$	-	-		-	d	-	-	-	-		-	d	-	-	-	-	-	-	1	0	0
$A_{n-1}B_{n-1}\bar{A}_{n-1}\bar{B}_{n-1}$	d	-		-	-	-	-	d	-		-	-	-	-	-	-	-	-	1	0	0
$A_1\bar{B}_1A_2B_2\bar{A}_2\bar{B}_2$	-	-		-	-	d	0	-	-		-	-	d	1	-	-	-	-	1	0	0
$A_1\bar{B}_1A_3B_3\bar{A}_3\bar{B}_3$	-	-		-	d	-	0	-	-		-	d	-	1	-	-	-	-	1	0	0
$\bar{A}_0B_0\bar{A}_0\bar{B}_0$	-	-		d	-	-	-	-	-		d	-	-	-	-	-	-	-	1	0	0
$A_{n-1}B_{n-1}\bar{A}_{n-1}\bar{B}_{n-1}$	d	-		-	-	-	-	d	-		-	-	-	-	-	-	-	-	1	0	0
$\bar{A}_{n-2}\bar{B}_{n-2}A_{n-1}B_{n-1}\bar{A}_{n-1}\bar{B}_{n-1}$	d	0		-	-	-	-	d	1		-	-	-	-	-	-	-	-	1	0	0
$A_{n-1}\bar{B}_{n-1}$	0	-		-	-	-	-	1	-		-	-	-	-	-	-	-	-	1	0	0
$ltA_0B_0\bar{A}_0\bar{B}_0$	-	-		-	-	-	d	-	-		-	-	-	-	d	-	-	1	0	0	1
$ltA_1B_1\bar{A}_1\bar{B}_1$	-	-		-	-	d	-	-	-		-	-	-	d	-	-	-	1	0	0	1
$A_1B_2\bar{A}_2\bar{B}_2$	-	-		-	-	d	-	-	-		-	-	d	-	-	-	-	-	0	0	1
$A_1B_3\bar{A}_3\bar{B}_3$	-	-		-	d	-	-	-	-		-	d	-	-	-	-	-	-	0	0	1
$A_{n-1}B_{n-1}\bar{A}_{n-1}\bar{B}_{n-1}$	d	-		-	-	-	-	d	-		-	-	-	-	-	-	-	-	0	0	1
$\bar{A}_0B_0A_1B_1\bar{A}_1\bar{B}_1$	-	-		-	-	-	1	-	-		-	-	-	-	0	-	-	-	0	0	1
$\bar{A}_0B_0A_2B_2\bar{A}_2\bar{B}_2$	-	-		-	-	-	1	-	-		-	-	-	-	0	-	-	-	0	0	1
$A_1B_1\bar{A}_1\bar{B}_1$	-	-		-	d	-	-	-	-		-	d	-	-	-	-	-	-	0	0	1
$A_{n-1}B_{n-1}\bar{A}_{n-1}\bar{B}_{n-1}$	d	-		-	-	-	-	d	-		-	-	-	-	-	-	-	-	0	0	1
$\bar{A}_0B_0A_1B_1\bar{A}_1\bar{B}_1$	-	-		-	-	-	1	-	-		-	-	-	-	0	-	-	-	0	0	1
$\bar{A}_0B_0A_2B_2\bar{A}_2\bar{B}_2$	-	-		-	-	-	1	-	-		-	-	-	-	0	-	-	-	0	0	1
$A_1B_1\bar{A}_1\bar{B}_1$	-	-		d	-	-	-	-	-		d	-	-	-	-	-	-	-	0	0	1
$A_{n-1}B_{n-1}\bar{A}_{n-1}\bar{B}_{n-1}$	d	-		-	-	-	-	d	-		-	-	-	-	-	-	-	-	0	0	1
$\bar{A}_{n-2}\bar{B}_{n-2}A_{n-1}B_{n-1}\bar{A}_{n-1}\bar{B}_{n-1}$	d	1		-	-	-	-	d	0		-	-	-	-	-	-	-	-	0	0	1
$\bar{A}_{n-1}\bar{B}_{n-1}$	1	-		-	-	-	-	0	-		-	-	-	-	-	-	-	-	0	0	1
$A_1B_1\bar{A}_1\bar{B}_1$	-	-		-	-	-	d	-	-		-	-	-	-	d	-	-	-	0	1	0
$A_1B_1\bar{A}_1\bar{B}_1$	-	-		-	-	-	d	-	-		-	-	-	-	d	-	-	-	0	1	0
$A_2B_2\bar{A}_2\bar{B}_2$	-	-		-	-	-	d	-	-		-	-	-	-	d	-	-	-	0	1	0
$A_3B_3\bar{A}_3\bar{B}_3$	-	-		-	-	-	d	-	-		-	-	-	-	d	-	-	-	0	1	0
$A_{n-1}B_{n-1}\bar{A}_{n-1}\bar{B}_{n-1}$	-	-		-	-	-	d	-	-		-	-	-	-	d	-	-	-	0	1	0

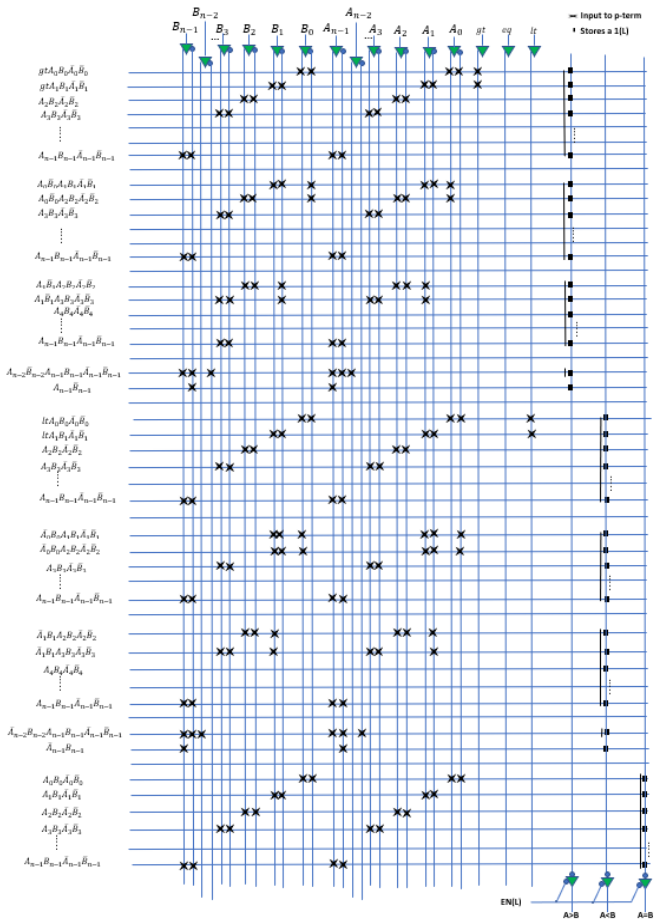


Figure 13. Symbolic representation of $8 \times p \times 3$ DMC FPLA programmed according to the p-term table in Figure 8. It shows the fusible bit position patterns in both the 'AND' and 'OR' planes

5 CONCLUSIONS

This paper proposes an FPLA network structure to behave as a speed optimised n-bit CDMC. The main contribution of the proposed method is that with the introduction of minimum or reduced SOP data, an efficient construction of CDMC is achieved which, ensures that the needed product terms fit within the FPLA's limited p-term capability.

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